Amendments to the Specification

Please replace the paragraph beginning on page 2, line 1, with the following rewritten paragraph:

The differences between SRAMs and DRAMs are fairly significant. For example, each cell of SRAM includes latch and pass transistors. Conversely, each cell of DRAM involves simply one transistor. While DRAMs are denser than SRAMs, DRAMs require additional support circuitry to coordinate the access of each cell, along with the need to periodically refresh that cell. The faster access time of SRAMs allow their use as the primary cache of the execution unit, whereas DRAMs are generally used as the main semiconductor memory. SRAMs are, therefore, placed on the same address and data bus as the execution unit, whereas DRAMs are linked to the execution unit by a memory controller and stand-alone memory bus.

Please replace the paragraph beginning on page 3, line 4, with the following rewritten paragraph:

One benefit of DDR is the higher speed at which data can be read from or written to the storage cells. Unfortunately, however, the ~~increases~~ increased speed of the I/O interface within the memory controller limits the available selection of available packing techniques. For example, when the data transfer rate exceeds several 100 MHz, relatively high inductance occur on the data signals sent to and from the memory controller. In an attempt to reduce the inductance, the data pins are kept as short as possible and are placed as close to the ground plane as possible. By shortening the data pins or leads extending from the controller and/or DRAMs and placing those pins near the ground plane, the current loop area and the magnetic flux are minimized. As described in "Circuits, Interconnections, and Packaging for VLSI," 1990, pg. 321 (herein incorporated by reference), packages which incur the poorest lead inductance are dual in-line packages (DIPs) or small outline packages (SOPs) which have approximately 3-50 nH inductance. Packages that have the smallest lead inductance (.025-1 nH) are those that employ flip-chip technology.

Please replace the paragraph beginning on page 6, line 12, with the following rewritten paragraph:

According to one embodiment, an integrated circuit is provided. The integrated circuit includes an execution engine, memory controller, or both an execution unit and a memory controller. The execution engine is preferably clocked at a first clock rate, and the memory controller is preferably clocked at a second clock rate. The second clock rate is desirably less than the first clock rate. A plurality of pins are configured on the integrated circuit and, preferably, extend from the integrated circuit as part of a lead frame. The pins are adapted to transfer data to and from the memory controller on both the rising and falling edges of the second clock signal transitioning at the second clock rate.

Please replace the paragraph beginning on page 14, line 17, with the following rewritten paragraph:

Specifically, the JEDEC standard for DDR transmissions calls out the stub-series terminated logic (SSTL) specification by which the various address and data bus pins are terminated at both controller 16 and external memory 12. The various features of SSTL_2 are described in the JEDEC standard, JEDEC Solid State Technology Association, December, 2000 (herein incorporated by reference). One benefit of the JEDEC standard is that the drivers and receivers are powered at a substantially reduced voltage value. For example, the voltage value for the data lines (DQ) is typically referred to as V_{DDQ}, which is defined to be ~~less~~ 2.5 volts or less. This allows for a lower power controller and memory device. The termination voltage or V_{TT} is essentially a reference voltage that is approximately equal to 1/2 of V_{DDQ}, for reasons described in the JEDEC standard.